A Software-Based Self-Test Methodology for On-Line Testing of Data TLBs

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***Abstract*— For small memory arrays that usually lack Memory Built-In Self-Test (MBIST), such as Translation Lookaside Buffer (TLB) arrays, Software-Based Self-Test (SBST) can be a flexible and low-cost solution for on-line March test application. In this paper, an SBST program development methodology is proposed for on-line testing of data TLB (D-TLB), both for data (SRAM) and tag (CAM) memory arrays. The SBST methodology exploits existing special purpose instructions that modern ISAs implement to access the TLBs for debug-diagnostic purposes, termed hereafter Direct TLB Access (DTA) instructions, as well as, the trap handler mechanism.**

I. INTRODUCTION

Most modern processors employ a small on-chip fully associative cache memory, commonly known as TLB to speed up the virtual memory translation. TLB arrays are small memory arrays that usually lack a MBIST scheme (e.g UltraSPARC T1 TLBs), since TLBs are limited size arrays (up to 128 entries).

Software-Based Self-Test (SBST) has recently emerged as a complementary solution for processor manufacturing and periodic on-line testing. In the case of on-line cache testing, SBST has increased flexibility to apply March tests [1]. Hence, SBST can be a viable solution for applying March tests to TLB arrays during on-line testing.

In this paper, we introduce an SBST program development methodology to apply March tests for on-line testing of both data (SRAM) and tag (CAM) D-TLB arrays. The methodology leverages the inherent power of moderns ISAs by exploiting special purpose instructions that we denote as Direct TLB Access (DTA) instructions and exploits the trap handler mechanism that is available in modern architectures, as well.

II. DTA INSTRUCTIONS IN MODERN ISAS

DTA instructions are special instructions for debug-diagnostic purposes that provide direct controllability and observability to TLB arrays and are suitable for SBST implementation of March tests that target D-TLBs. An ideal DTA instruction contains these fields:

- TLB Line Selection (*LS*) field
- Write/Read/Compare operation (*WRC*) selection field
- Array Selection (*AS*) field
- From/To data Address (*A*) field

In practice such an ideal DTA instruction is not present in ISAs but it can be indirectly implemented by combining a set of existing DTA instructions that should cover in total all fields of the ideal one.

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III. D-TLB SBST METHODOLOGY

The SBST methodology implements low cost SBST March tests that target D-TLB arrays by taking advantage of existing DTA instructions in modern ISAs. If the ISA lacks DTA instructions, the methodology exploits the native TLB miss & refill mechanism along with the trap handler mechanism to implement the March write read and compare operations.

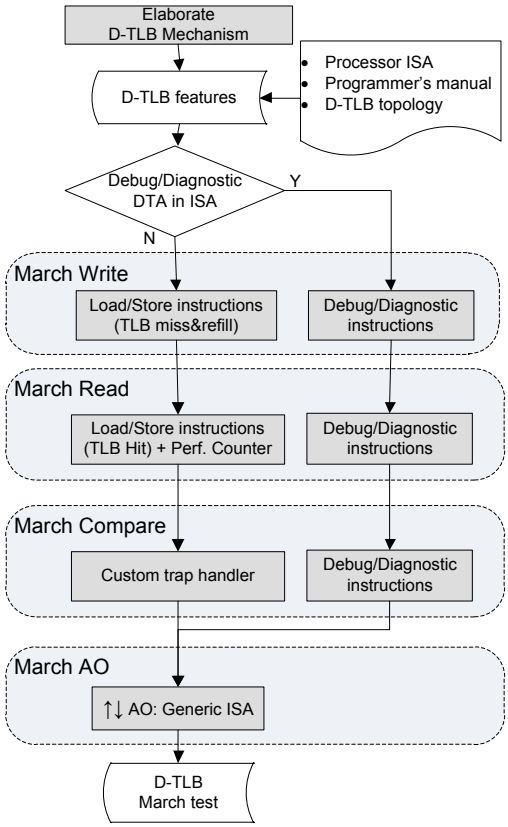

Figure 1: SBST methodology for D-TLB arrays

The SBST methodology has been applied to the D-TLB arrays of OpenSPARC T1 processor. We have implemented a set of contemporary March tests for both storage and comparison faults. Experimental results show a significant improvement in test time (on average 40%) for all the applied March tests when such debug-diagnostic instructions are exploited while preserving the March test quality.

REFERENCES

[1] G. Theodorou, N. Kranitis, A. Paschalis, D. Gizopoulos, "A Software-Based Self-Test Methodology for On-Line Testing of Processor Caches", in Proc. of *Int'l Test Conference (ITC)*, 2011